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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/808,884 | 03/14/2001 | Eric John Hewitt | AHA-02101 | 5252 |

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| EXAMINER | |
|---|---|
| TORRES, JOSEPH D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2133 | |

DATE MAILED: 12/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/808,884 | HEWITT ET AL. | |
| | Examiner | Art Unit | |
| | Joseph D. Torres | 2133 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *1-10 and 23-40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election with traverse of Claims 11-22 in the reply filed on 05/05/2005 is acknowledged. The traversal is on the ground(s) that "As the classifications for the claims remain unchanged since the first Restriction Requirement, there is no reason that this Restriction Requirement, even if warranted, could not have been made previously". This is not found persuasive because the Examiner has provided additional classification for the newly restricted claims and the restriction is warranted because the Applicant is entitled to two searches in an application. A second search has not been concluded for any of the non-elected claims. The Applicant claims that 1-7 and 11-40 are allowable. If that were so, the Examiner would have to search all of the Applicant's inventions to verify it.

The requirement is still deemed proper and is therefore made FINAL.

Claims 1-7 and 23-40 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 05/05/2005.

This application contains claims 1-7 and 23-40 drawn to nonelected inventions with traverse. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 11-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Glover; Neal et al. (US 4564945 A, hereafter referred to as Glover) in view of Rhines; Don S. et al. (US 5392299 A, hereafter referred to as Rhines).

35 U.S.C. 103(a) rejection of claim 11.

Glover teaches receiving a row of the block and immediately outputting the row encoding the information bits in the row, wherein a first set of encoded data is

generated according to a first encoding scheme and outputting the first set of encoded data (col. 4, lines 9-12 in Glover teach that first row encoding is performed on an array according to a first Reed-Solomon encoding scheme; Note: performing Reed-Solomon encoding on rows clearly suggests a first Reed-Solomon encoder for receiving and encoding the rows and outputting the encoded rows for subsequent processing); encoding the information bits in a column according to a second encoding scheme, wherein a second set of encoded data is generated and iteratively updated according to the information bits in the row (col. 4, lines 11-14 in Glover teach that column encoding is performed on the row encoded array according to a second Reed-Solomon encoding scheme; Note: col. 4, line 14 teaches that the same process for row and column encoding an array is performed for 30 data array blocks which clearly suggest the iterative use of the row and column encoding to produce a 3-dimensional block comprising 30 row and column encoded arrays); block encoding the information bits in the block according to a parity encoding scheme, wherein a set of encoded data is generated according to the information bits in the row and column and the first and second sets of encoded data; outputting the second set of encoded data after all the information bits and all subsequent first sets of encoded data are outputted; and outputting the set of encoded data (col. 4, lines 14-19 in Glover teaches that the 3-dimensional block comprising 30 row and column encoded arrays is block encoded to produce two additional redundancy arrays; Note: performing Reed-Solomon encoding on the 3-dimensional block comprising 30 row and column encoded arrays clearly suggests a first Reed-Solomon encoder for receiving and encoding the 3-dimensional

block comprising 30 row and column encoded arrays and outputting the 3-dimensional block comprising 30 row and column encoded arrays for subsequent processing) However Glover does not explicitly teach the specific use of hyper-diagonally encoding. Rhines, in an analogous art, teaches use of hyper-diagonally encoding (Figure 4A, 4B and 5 teach hyper-diagonally encoding).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Glover with the teachings of Rhines by including use of hyper-diagonally encoding. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of hyper-diagonally encoding would have provided protection against burst errors (Abstract, Rhines).

35 U.S.C. 103(a) rejection of claims 12 and 13.

Claims 12 and 13 provide alternative embodiment for claim 11, in particular, using different coding schemes. The Examiner asserts that the triple orthogonal interleaved error correction system using a hyper diagonal encoder taught in Rhines is only an exemplary embodiment of triple orthogonal interleaved error correction systems and that rearranging the exemplary embodiment of the triple orthogonal interleaved error correction system taught in Rhines to produce an alternative embodiment whereby the first encoder in the set of serially concatenated encoders is a row encoder, the second encoder is a column encoder and the third encoder is a hyper encoder is an obvious

alternative embodiment as Rhines states in col. 25, col. 34-42 in Rhines since such a rearranged encoder is still a triple orthogonal interleaved error correction system.

35 U.S.C. 103(a) rejection of claim 14.

Figures 4A, 4B and 5 in Rhines teach that the block of data is three-dimensional.

35 U.S.C. 103(a) rejection of claim 15.

Hyper encoding is a third encoding scheme; hence C2 error correction 90 of Figure 2 in Rhines is a third encoding scheme. Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder

35 U.S.C. 103(a) rejection of claim 16.

Rhines teaches that the C2 parity is a separate 3-d hyper-plane from the User Data 3-d block added to the User Data array in Figure 8.

35 U.S.C. 103(a) rejection of claim 17.

Figure 13A in Rhines teaches the first set of encoded data is stored in a row encode storage array, wherein the row encode storage array includes a plurality of row array bits.

35 U.S.C. 103(a) rejection of claim 18.

Glover and Rhines substantially teaches the claimed invention described in claims 11-14 (as rejected above).

However Glover and Rhines does not explicitly teach the specific use of resetting the row encode storage array such that all row array bits are set to zero, wherein the step of resetting is executed after the first set of encoded data is outputted.

The Examiner asserts that the values of the C2 parity bits of Figures 4A, 4B and 5 in Rhines does not matter since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Glover and Rhines by including use of resetting the row encode storage array such that all row array bits are set to zero after the first set of encoded data is outputted and before the step of performing the parity calculation along the hyper diagonal is executed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of resetting the row encode storage array such that all row array bits are set to zero after the first set of encoded data is outputted and before the step of performing the parity calculation along the hyper diagonal is executed would not have mattered since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

35 U.S.C. 103(a) rejection of claim 19.

Figure 13A in Rhines teaches the first set of encoded data is stored in a row encode storage array, wherein the row encode storage array includes a plurality of row array bits.

35 U.S.C. 103(a) rejection of claim 20.

Figure 4B in Rhines teaches the hyper set of encoded data is stored in a hyper parity array, wherein the hyper parity array includes a plurality of parity array bits.

35 U.S.C. 103(a) rejection of claim 21.

Col. 4, lines 59-62 and col. 10, lines 31-68 in Rhines teach that prior to generating the C2 error correction 90 of Figure 2 in Rhines, the rows of the first series of data planes 40, 42 and 44 in Figures 4A and 5 are orthogonally shuffled by the outer Interleaver 16 so that the new block of Figure 4B is formed whereby the x-y planes of the new block of Figure 4B are the diagonal planes of the Block in Figure 4A; hence the column encoding of the new block of Figure 4B to from the C2 error correction of Figures 2 and 8 is equivalent and is a means for performing a parity calculation along a hyper diagonal in the Block in Figure 4A, wherein a parity result for the C2 parity calculation of Figure 8 is generated; Note: the Middle C2 encoder must iteratively receive user data information bits in hyper columns since Middle C2 hyper column encoder 90 in Figure 2 is a hyper column encoder.

35 U.S.C. 103(a) rejection of claim 22.

Glover and Rhines substantially teaches the claimed invention described in claims 11-14 (as rejected above).

However Glover and Rhines does not explicitly teach the specific use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed.

The Examiner asserts that the values of the C2 parity bits of Figures 4A, 4B and 5 in Rhines does not matter since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

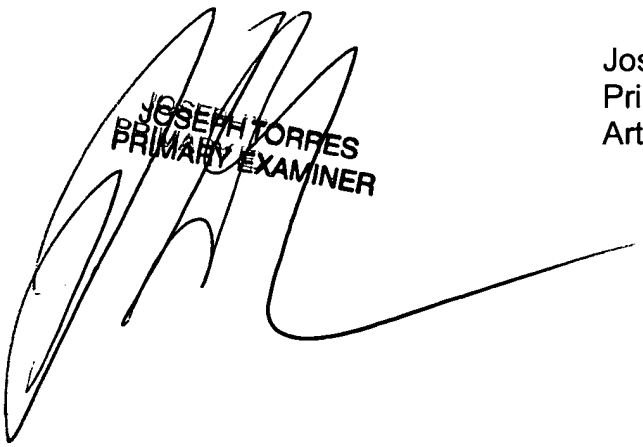
Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Glover and Rhines by including use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of initializing the parity array such that the parity bits are set to zero before the step of performing the parity calculation along the hyper diagonal is executed would not have mattered since any previous values would be discarded and replaced with newly calculated C2 parity bits because the current C2 parity bits only depend on the current calculation.

***Conclusion***

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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